

Printed wire panel of master control is tested at left. Overall view of right shows hand-wired redundancy able in center

# COMPUTER Selects

**SUMMARY** — Premium savings bond plan operating in England requires that over 10,000 prize-winning numbers be randomly selected monthly from over 100 million bond numbers. Computer ERNIE, (Electronic Random Number Indicating Equipment) uses noise generators combined with counters and storage systems to provide a printed list of purely random bond numbers. Circuits use transistors, ferrite-core binaries and printed wiring techniques

**L**OTTERIES in England were discontinued in 1826. Current introduction of a state lottery would be opposed by considerable public opinion. However, the plan of using Premium Savings Bonds is not a lottery in that the purchasers' capital investment is not at stake. An element of chance is introduced in the distribution of interest earned by the investment.

The chance of being a prize winner works out at about 1 in 2,000 for the first draw and at better than 1 in 12,000 in each subsequent monthly draw.

Bonds are issued in 23 denominations from 1 to 500 units and participants can enter the plan at any

time, increase their stake or withdraw all or part of it at any time. A 50-unit bond has 50 chances of winning just as do 50 1-unit bonds. Winners are not withdrawn from subsequent draws.

### Number Selection

Owing to these conditions and also to the very large numbers involved (nearly 50 million units were sold in Nov. 1956), it was decided that the draws could be best carried out by an electronic computer, supplemented by manual operations thereafter.

For each denomination of bonds there is a potential numbering range of 100 million; the total num-

bers for the plan is therefore 2,300 million, approximately equal to the world population. For the Nov. sales, the numbered bonds ranged up to 30 million for one denomination. Accordingly ERNIE is adjusted to generate  $23 \times 30 = 690$  million numbers.

A typical bond number is 2 AZ 987654, a coded form for bond number 20,987,654 of £1 denomination. Multiple units have consecutive numbers and bear the first and last number concerned. The selection of prize winners must, therefore, be made from 690 million 9-digit numbers. Of these digits the first is in a scale of 3 (the second 23, the remainder in a scale of 10.

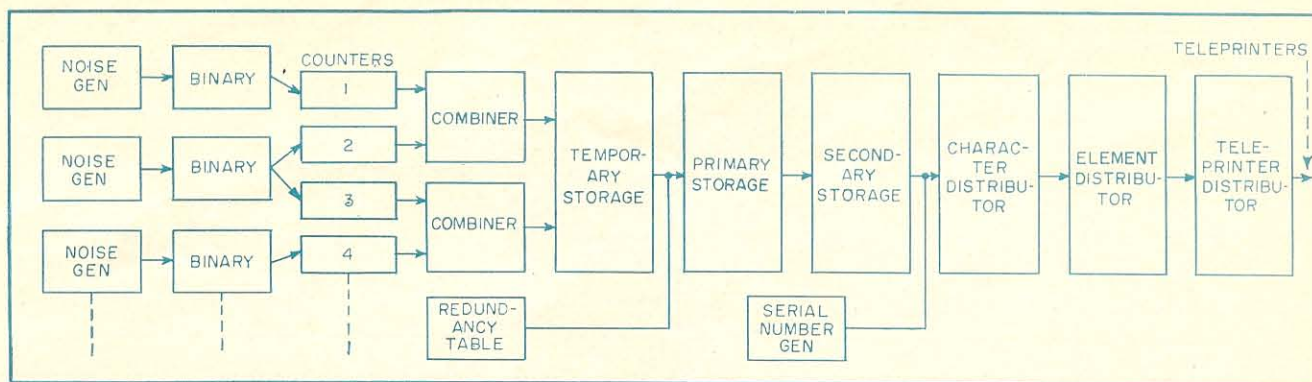


FIG. 1—Block diagram of ERNIE. Ten noise generators are used rather than nine to ensure that the machine operates when one generator fails.

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# Premium Bond Winners

For the first draw nearly 60,000 numbers must be printed, but of these only some 23,000 will be eligible. This discrepancy arises because the bonds are sold at thousands of offices, and at any one time many bonds are in stock awaiting sale. Consequently the numbering ranges of eligible bonds are broken. The computer rejects blocks of unsold bonds when these amount to 100,000 or more, but it is uneconomical for it to deal with smaller blocks.

## Generation of Random Numbers

Each of the 9 digits of the bond number is generated from a separate noise source that consists of a neon diode passing a steady current. This noise is amplified and applied to a bottom clipper. Its output triggers a monostable multivibrator which generates pulses of standard amplitude and width with a minimum time separation between pulses.

These standard pulses, randomly spaced in time, drive a single-stage binary. Its two outputs in turn drive a counter.

The counters are in scales of 6,

24 or 10 since counters must be even in scale. The scale of six is converted later to a scale of three and then used for the first digit. One digit from the scale of 24 is suppressed, leaving a scale of 23 for the demonstration digit.

The rate of pulse generation is sufficient to cause the counters to make several complete revolutions in one-sixth of a second. At the end of this period the noise generator output is suppressed and the counters are read.

Fault conditions leading to a cyclic component in a noise generator and amplifier may lead to a nonrandom result not readily detected. This event is made much less likely by separately generating each digit or letter from two random noise generators each driving an independent counter. When the counters are stopped the outputs of each pair are combined by subtracting one number from the other and the result is still random.

Noise generators are shared between counters as shown in the block diagram of Fig. 1 so each combiner works from two different noise generators. It is useful to

provide 10 rather than the minimum of 9 noise generators, because if one out of nine failed, it would prevent the satisfactory operation of the machine.

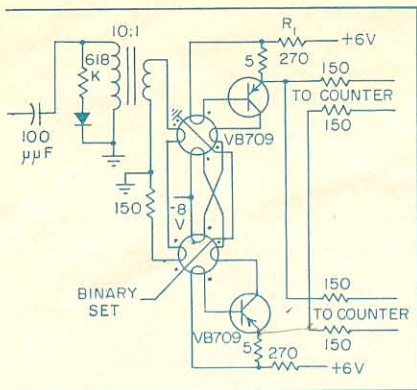
## Redundant Number Suppression

Redundancy arises in two ways: intermediate and terminal. The intermediate redundancy, arising from unsold bonds in the selling offices, has already been described. Terminal redundancy is the more important and refers to those bonds which have never been issued to a selling office. The sales of each denomination vary widely but the machine generates 30 million numbers for each. If only 15.3 million have been issued, then there is a terminal redundancy of 14.7 million for this denomination.

The terminal redundancy is dealt with to the next complete multiple of 100,000 greater than the highest eligible number issued in a bond denomination. Thus the first four digits of a generated number require examination.

The number of combinations offered to the suppression device, called the redundancy table, is 300





pulses to appear alternately at emitters counting circuit during readout

Amplified noise signals thus appear on the grid of  $V_4$ , the control-grid bias of which is adjusted by fixed resistors to some  $-20$  volts. Only voltage peaks which equal or exceed the bias can cause  $V_4$  to conduct. The mean rate (over a period of several minutes) of the output pulses is made about 3,000 a second by adjusting the bias.

Pulses from  $V_4$  are applied through a diode gate to a monostable multivibrator formed by  $V_5$  and  $V_6$ . Tube  $V_6$  is normally non-conducting and  $V_5$  and diode  $D_1$  conducting. A negative input pulse from the amplifier is transmitted through  $D_1$  to the anode of  $V_6$  and through a capacitor to the grid of  $V_5$ , triggering  $V_6$  into conduction. Diode  $D_1$  is now reverse biased and remains so for the  $20\text{-}\mu\text{sec}$  restoring time. Diode  $D_1$  prevents any input signal from triggering until the anode of  $V_6$  is substantially back to its normal voltage.

The binary circuit has two transistors and two rectangular hysteresis loop ferrite cores. The output pulse from  $V_6$  is differentiated and applied via a 10 to 1 step-down transformer to a multiturn winding on each of the two cores. Initially the two cores have been set to opposite states by current passed through the binary-set wire. The incoming pulse therefore resets one of the cores, and the resulting large change of flux from one remnant condition to the other induces a voltage on each of the windings on the core.

One winding, connected between base and emitter of the associated transistor, causes it to conduct. Col-

lector current flows through a feedback winding on the core to assist the switching action. At the same time current flows through a winding on the second core to set it. Emitter current flowing through a resistor provides a 12-volt negative-going pulse for  $5\ \mu\text{sec}$  to one phase lead ( $\phi_1$ ) of the following counters. The other transistor produces no output as it is already cut off.

The result of this operation is that the state of the two cores has been transposed and an output pulse produced. Since the circuit is symmetrical a second input pulse will return both cores to their original state and provide a pulse from the other transistor on the second phase lead ( $\phi_2$ ). A series of pulses from the noise generator will thus cause negative pulses to appear alternately at the emitters of the two transistors. Switching off a transistor is made more rapid by the voltage developed by the emitter current flowing through the resistor connected between base and emitter.

The noise generators are switched off at intervals of 160 millisecond by blanking pulses of 4 millisecond duration applied to the suppressor grid of  $V_4$ . During the latter period the random signals cannot affect the counters, thus allowing reading of their count. The mean count per interval is about 500. The statistical distribution of the source is adequate to ensure that any final position of a single stage decimal or 24-way counter is equally likely, assuming also that a

random starting position is used. This latter condition is ensured by starting the counter from its previous stopping position.

Provision is made for injecting a predetermined number of pulses into the monostable multivibrator at the grid of  $V_6$ . These pulses are used during the blanking period to operate the counter combiner.

### Counters and Combiner

The circuit of the two counters and the combiner used in generating the first digit is shown in Fig. 3. Cores  $X_1$  to  $X_6$  with their associated transistors  $Q_1$  to  $Q_6$  form counter A. The pulses to be counted are applied alternately to transistors  $Q_{14}$  and  $Q_{15}$ , switching these and resulting in current pulses through the series-connected  $\phi_1$  windings on cores  $X_1$ ,  $X_3$  and  $X_5$  and the  $\phi_2$  windings on cores  $X_2$ ,  $X_4$  and  $X_6$  alternately.

The counter is initially set up with one core in the set condition and all others reset. If core  $X_2$  is set, then the first pulse on the  $\phi_2$  lead will reset this core. The voltage induced in winding  $N_1$  exceeds the positive bias of  $0.75\text{v}$  and carries the base of transistor  $Q_2$  negative with respect to its emitter, causing the transistor to switch rapidly to the highly conducting condition. The resulting collector current, defined by  $R_1$  and the supply voltage and flowing in winding  $N_2$  of core  $X_3$ , sets this core and so completes the transfer of the condition originally stored on  $X_2$ .

Each successive pulse causes a

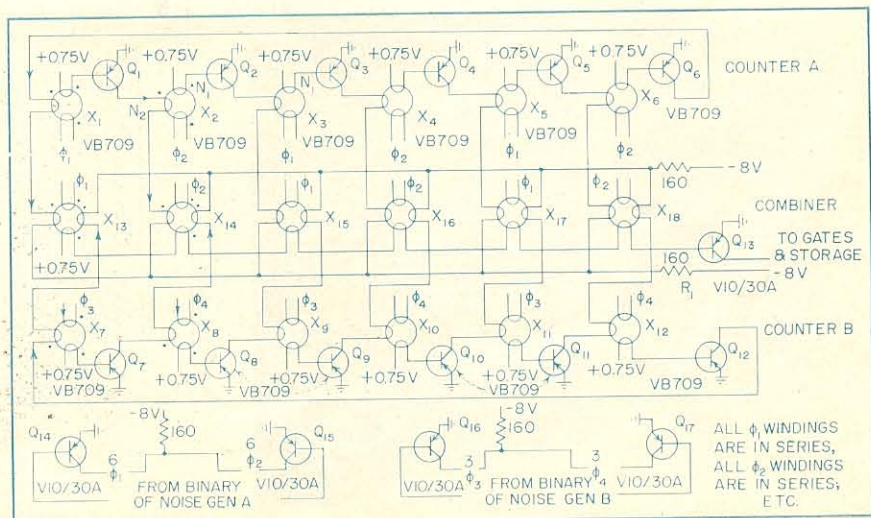


FIG. 3—Transistors and ferrite cores make up all counter and combiner circuits. Transistor coupling reduces pulse power required by deriving current from another source

further transfer in the same manner. During the resetting of  $X_2$  a voltage is induced in winding  $N_2$ , but since this winding is connected in series with  $Q_1$  which is in the nonconducting condition, no current flows in the circuit. The only power required from the drive pulse is that required to reset the core plus that required to bottom the transistor. The time required for the core to reset is longer than that required to switch an unloaded core due to the load imposed by the transistor base circuit.

The change of flux when core  $X_3$  is set induces voltages in the transistor base winding  $N_1$  and the  $\phi_1$  drive winding. These are in the opposite sense to those induced during resetting, hence the transistor base is driven further positive with respect to its emitter. The resulting current in the  $N_1$  winding is therefore negligible. The drive circuit transistor is nonconducting so no current can flow in this circuit either. The core is effectively unloaded and this ensures that it is set more rapidly than the loaded core  $X_2$  can be reset.

### Transistor Coupling

Use of a transistor as a coupling between the two cores has two advantages. It ensures that currents flow only where required to perform a useful function and, by deriving the transfer current from a separate source, greatly reduces the pulse power required. No power is

used between counts. Since each transistor conducts only when transferring information from one stage to the next and this occurs once per revolution of the counter, the mean dissipation of the transistors may be kept to a low value. When used as a counter the circuit described may use one collector resistor common to all stages. If separate resistors are used for each stage the circuit may be used as a two-core-per-bit register.

Cores  $X_7$  to  $X_{12}$  with transistors  $Q_7$  to  $Q_{12}$  form counter  $B$ , operating in an exactly similar manner from pulses delivered by the second noise source. Cores  $X_{13}$  to  $X_{18}$  form the combiner, giving an output pulse to switch transistor  $Q_{13}$  at a time characteristic of the combined counts.

### Resetting

The lead from  $Q_1$  which sets the following core  $X_2$  is extended through a winding on  $X_{14}$  and sets this core at the same time as  $X_2$ . The resetting pulse  $\phi_3$ , connected to  $X_2$ , is also connected to a resetting winding on  $X_{14}$ . The other combiner cores are associated in a similar manner with corresponding counter  $A$  cores. In the absence of any other signals to  $X_{13}$  to  $X_{18}$  this ensures that these cores are set and reset in synchronism with the corresponding cores in counter  $A$ .

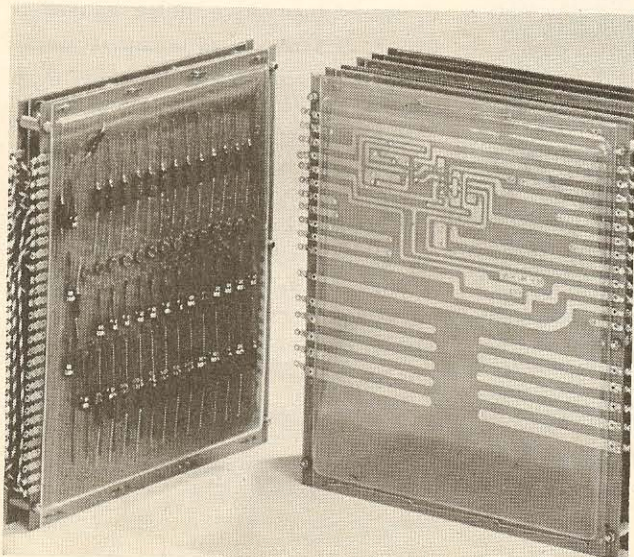
A further resetting winding on each combiner core is connected in series with the setting winding of

the associated core in counter  $B$  and thus each transfer of counter  $B$  results in an attempt to reset one of the combiner cores. Output windings on each core are series-connected between a positive bias potential and the base of transistor  $Q_{13}$  so that during the resetting of each combiner core this transistor is switched to the conducting condition.

### Combining Action

Every 160 milliseconds the noise generators are blanked off and the recorded  $A$  and  $B$  counts have to be combined. One combiner core will be in a set condition unless counter  $B$  has overtaken counter  $A$  immediately prior to the blanking pulse, in which case all combiner cores will be reset. A single pulse is first applied by the master control to counter  $A$ . The resulting transfer ensures that one of the combiner cores is set. A train of pulses is then applied to counter  $B$ , the number of pulses being sufficient to cause this to complete at least one complete cycle.

As one of the transfers of this counter takes place the set combiner core will be reset. The resulting output pulse will switch transistor  $Q_{13}$ . This occurs after a number of pulses equal to one plus the difference between the recorded  $B$  and  $A$  counts. For example, assume counter  $A$  records 4 and counter  $B$  2, so that cores  $X_1$  and  $X_2$  are set. The single  $A$  pulse causes



Printed circuit sandwiches show how ferrite cores and transistors are mounted. Molded plastic covers protect both sides of board

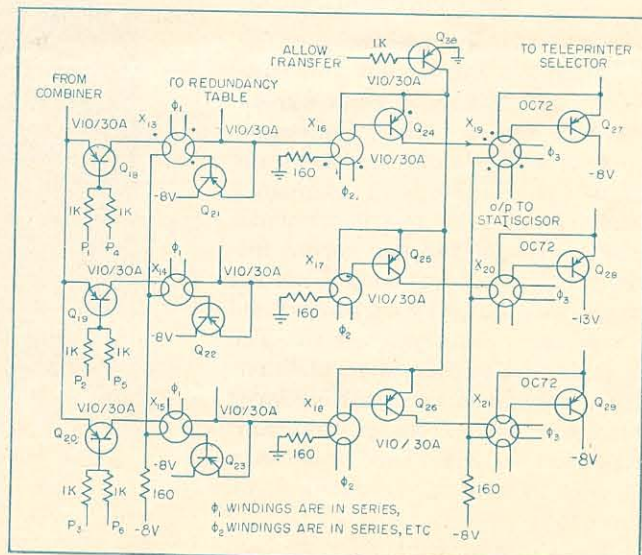
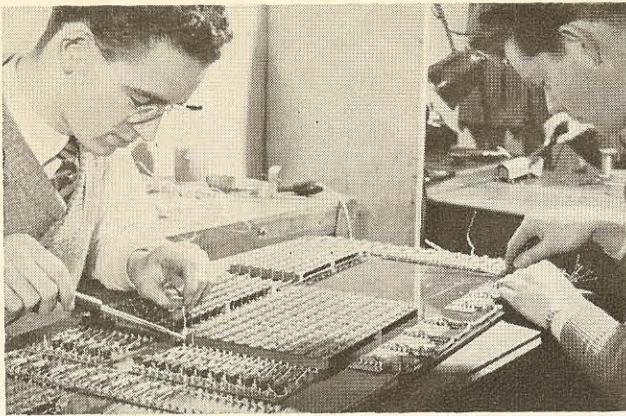
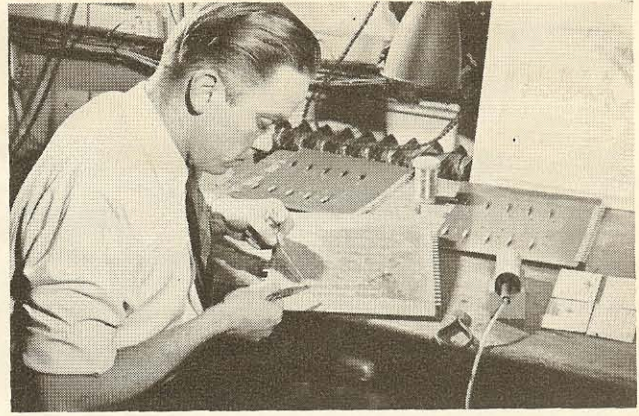


FIG. 4—Storage circuits associated with first digit of bond number. Basically, storage circuits linked with other digits are similar



Several connections on redundancy table must be changed for each draw to include bond numbers issued since previous draw



Printed wiring boards are equipped by hand. Terminals at end permit rewiring to provide other counter and storage facilities

$X_5$  and  $X_{17}$  to be set and  $X_{17}$  will be reset by the third  $B$  pulse:  $4 - 2 + 1 = 3$ .

### Storage Circuits

The number of pulses required to obtain the output pulse from the combiner is counted and recorded in temporary storage, examined in conjunction with other digits in the redundancy table, and if not indicated as redundant, is finally transferred to storage for printing by the appropriate teleprinters.

The storage circuits associated with the first digit are shown in Fig 4. Transistors  $Q_{13}$  to  $Q_{20}$  operate as gates. When made conducting by negative pulses applied to their bases, they connect the setting windings of temporary storage cores  $X_{13}$  to  $X_{16}$  to the output from  $Q_{13}$  of the combiner.

The pulses are applied sequentially in synchronism with the pulses of the counter  $B$  train and thus result in the setting of the core corresponding to the combination of the two counters. Two pulses are applied to each gate and the scale of six employed in the counters and combiners is stored in a scale of three as required for the first digit of the bond numbers.

After the counter  $B$  pulse train is complete, all temporary storage cores are reset by a pulse from the master control and the marked core gives a pulse which switches its associated coupling transistor  $Q_{21}$ ,  $Q_{22}$  or  $Q_{23}$ . Each transistor has its collector connected to the negative supply, with the setting winding of the corresponding primary storage core  $X_{16}$  to  $X_{18}$  in series with a re-

sistor between emitter and ground. When the temporary storage cores are reset, the corresponding primary storage core is set and an 8-volt negative pulse from the emitter of the coupling transistor is sent to the redundancy table.

The transfer from temporary to primary storage occurs simultaneously for all digits, in contrast with the transfers from combiners to temporary storage which occur at times determined by the combinations. Thus simultaneously pulses indicating the first four digits are sent to the table for comparison with the stored pattern.

If the table indicates that the number being offered is redundant then the primary storage cores of all digits are reset immediately. The base of transistor  $Q_{20}$  is held at a positive potential so, although one of the coupling transistors  $Q_{24}$  to  $Q_{26}$  will be switched, its collector current will be negligible and the code will be erased.

If no redundancy is signaled to the master control, resetting of the primary storage cores is delayed until printing of the previous message has been completed. The secondary storage cores  $X_{19}$  to  $X_{21}$  are then known to be reset, and resetting of the primary storage cores accompanied by a negative allow-transfer pulse to the base of  $Q_{20}$  transfers the code to the appropriate secondary storage core. From here it is transferred digit by digit, interleaved with letter and figure shift signals, to a statiscisor employing cold-cathode triodes, translated to teleprinter code and transmitted to the printers.

While a printable number is held in the primary storage waiting for the printing of the previous message to be completed the periodic blanking of the noise generators continues. To prevent further numbers being passed to the occupied storage, the gating pulses and the pulses to the  $A$  and  $B$  binary units are inhibited by the master control.

To arrange for the teleprinter switching, transistors  $Q_{27}$  to  $Q_{29}$  are switched by the voltage generated as the associated core is set. The emitter current causes a relay to operate and connect the required teleprinters to the line. To avoid undue slowing of the setting of secondary storage cores, transistors  $Q_{27}$  to  $Q_{29}$  and their drive windings are chosen to reflect the minimum possible load to the drive circuit.

Basically the storage circuits associated with all other digits are similar. For all digits but the first, the storage scale is the same as that in the counters and only one pulse is applied.

The redundancy table circuit requires a positive pulse from the second digit. To obtain this the loads are connected in the collector circuits instead of in the emitter circuits of the transistors coupling temporary storage to primary storage. Finally, the selection of the teleprinters depends on the first two digits only so transistors  $Q_{27}$  to  $Q_{29}$  are omitted from the circuits generating other digits.

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